

Claims

What is claimed is:

1. An information handling system comprising:
 - a first node for:
 - detecting a first memory in the first node;
 - detecting a second memory in a second node coupled to the first node;
 - ensuring that a first set of contiguous addresses is mapped to a portion of the first memory, the first set of contiguous addresses each having a value lower than a four gigabyte address; and
 - ensuring a second set of contiguous addresses is mapped to a portion of the second memory, the second set of contiguous addresses each having a value lower than the four gigabyte address.
2. The information handling system of claim 1, wherein the first node is for:
 - reserving a third set of contiguous addresses that each have a value lower than the four gigabyte address.
3. The information handling system of claim 2, wherein the first node is for:
 - detecting a third memory in a third node coupled to the first node subsequent to the first node and the second node being booted; and
 - mapping the third set of contiguous addresses to a portion of the third memory.
4. The information handling system of claim 1, wherein the first node is for:
 - detecting a size of the first memory in the first node; and

3 determining a size of the portion of the first memory in
4 response to the size of the first memory.

1 5. The information handling system of claim 4, wherein the first node is for:
2 detecting a size of the second memory in the second node; and
3 determining the size of the portion of the first memory and a
4 size of the portion of the second memory in response to the size of the
5 first memory and the size of the second memory.

1 6. The information handling system of claim 1, wherein the first node is for:
2 detecting a number of nodes that are coupled to the first node; and
3 determining a size of the portion of the first memory in response
4 to the number of nodes.

1 7. The information handling system of claim 1, wherein the first node is for:
2 detecting a maximum number of nodes that may be coupled to the first
3 node; and
4 determining a size of the portion of the first memory in response
5 to the maximum number of nodes.

1 8. A method comprising:
2 detecting a first memory in a first node;
3 detecting a second memory in a second node coupled to the first
4 node;
5 ensuring that a first set of contiguous addresses is mapped to a
6 portion of the first memory, the first set of contiguous addresses each having
7 a value lower than a four gigabyte address; and
8 ensuring a second set of contiguous addresses is mapped to a

9 portion of the second memory, the second set of contiguous
10 addresses each having a value lower than the four gigabyte address.

1 9. The method of claim 8, further comprising:
2 reserving a third set of contiguous addresses that each have a
3 value lower than the four gigabyte address.

1 10. The method of claim 9, further comprising:
2 detecting a third memory in a third node coupled to the first node
3 subsequent to the first node and the second node being booted; and
4 mapping the third set of contiguous addresses to a portion of
5 the third memory.

1 11. The method of claim 8, further comprising:
2 detecting a size of the first memory in the first node; and
3 determining a size of the portion of the first memory in
4 response to the size of the first memory.

1 12. The method of claim 11, further comprising:
2 detecting a size of the second memory in the second node; and
3 determining the size of the portion of the first memory and a
4 size of the portion of the second memory in response to the size of the
5 first memory and the size of the second memory.

1 13. The method of claim 8, further comprising:
2 detecting a number of nodes that are coupled to the first node; and
3 determining a size of the portion of the first memory in response
4 to the number of nodes.

1 14. The method of claim 8, further comprising:
2 detecting a maximum number of nodes that may be coupled to the first
3 node; and
4 determining a size of the portion of the first memory in response
5 to the maximum number of nodes.

1 15. A computer program product comprising:
2 a computer program processable by a first node to:
3 detect a first memory in the first node;
4 detect a second memory in a second node coupled to the first
5 node;
6 ensure that a first set of contiguous addresses is mapped to a
7 portion of the first memory, the first set of contiguous addresses each
8 having a value lower than a four gigabyte address; and
9 ensure a second set of contiguous addresses is mapped to a
10 portion of the second memory, the second set of contiguous
11 addresses each having a value lower than the four gigabyte address;
12 and
13 an apparatus from which the computer program is accessible by
14 the first node.

1 16. The computer program product of claim 15, wherein the computer program is
2 processable by the first node to:
3 reserve a third set of contiguous addresses that each have a
4 value lower than the four gigabyte address.

1 17. The computer program product of claim 16, wherein the computer program is
2 processable by the first node to:

3 detect a third memory in a third node coupled to the first node
4 subsequent to the first node and the second node being booted; and
5 map the third set of contiguous addresses to a portion of the
6 third memory.

1 18. The computer program product of claim 15, wherein the computer program is
2 processable by the first node to:

3 detect a size of the first memory in the first node; and
4 determine a size of the portion of the first memory in
5 response to the size of the first memory.

1 19. The computer program product of claim 18, wherein the computer program is
2 processable by the first node to:

3 detect a size of the second memory in the second node; and
4 determine the size of the portion of the first memory and a size
5 of the portion of the second memory in response to the size of the first
6 memory and the size of the second memory.

1 20. The computer program product of claim 15, wherein the computer program is
2 processable by the first node to:

3 detect a number of nodes that are coupled to the first node; and
4 determine a size of the portion of the first memory in response
5 to the number of nodes.

1 21. The computer program product of claim 15, wherein the computer program is
2 processable by the first node to:

3 detect a maximum number of nodes that may be coupled to the first
4 node; and

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5 determine a size of the portion of the first memory in response
6 to the maximum number of nodes.

1 22. The computer program product of claim 15, wherein the computer program
2 comprises a basic input output system (BIOS).